AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (currently amended): A method of forming a bit line contact via, comprising:

providing a substrate with a transistor thereon, the transistor having a gate electrode, drain region, and source region;

forming a conductive layer overlying the drain region, wherein the top surface of the conductive layer is lower than that of the gate electrode;

conformally forming an insulating barrier layer overlying the substrate;

blanketly forming a dielectric layer overlying the insulating barrier layer; and

forming a via through the dielectric layer and insulating barrier layer, exposing the conductive layer.

Claim 2 (currently amended): The method as claimed in claim 1, wherein forming the conductive layer further comprises:

blanketly forming ~~the conductive layer~~ a layer of conductive material overlying the substrate;

removing ~~the unwanted~~ a portion of the conductive material layer, leaving a conductive layer ~~thinner than the gate electrode,~~ overlying the drain region and source region, wherein the top surface of the conductive layer is lower than that of the gate electrode;

forming a patterned resist layer exposing the conductive layer overlying the source region;

removing the exposed conductive layer using the patterned resist layer as a mask; and

removing the patterned resist layer.

Claim 3 (currently amended): The method as claimed in claim 1, wherein forming the conductive layer further comprises:

conformally forming a metal/metal compound layer overlying the substrate;

blanketly forming ~~the conductive layer~~ a layer of conductive material overlying the substrate;

removing ~~the unwanted~~ a portion of the conductive material layer, ~~remaining~~ leaving the conductive layer~~, thinner than the gate electrode,~~ overlying the drain region and source region, wherein the top surface of the conductive layer is lower than that of the gate electrode;

forming a patterned resist layer exposing the conductive layer overlying the source region;

removing the exposed conductive layer using the patterned resist layer as a mask and the metal/metal compound layer as a stop layer, thereby exposing the metal/metal compound layer overlying the source region; and

removing the patterned resist layer and exposed metal/metal compound layer.

Claim 4 (currently amended): The method as claimed in claim 1, wherein forming the conductive layer further comprises:

conformally forming a Ti/TiSi layer overlying the substrate;

blanketly forming ~~the conductive layer~~ a layer of conductive material overlying the substrate;

removing ~~the unwanted~~ a portion of the conductive material layer, leaving the conductive layer ~~thinner than the gate electrode,~~ overlying the drain region and source region, wherein the top surface of the conductive layer is lower than that of the gate electrode;

forming a patterned resist layer exposing the conductive layer overlying the source region;

removing the exposed conductive layer using the patterned resist layer as a mask and the Ti/TiSi layer as a stop layer, thereby exposing the Ti/TiSi layer overlying the source region;

ashing the patterned resist layer using oxygen plasma; and

removing the exposed metal/metal compound layer using SPM (sulfuric acid-hydrogen peroxide mixture) and APM (ammonium hydrogen peroxide mixture).

Claim 5 (original): The method as claimed in claim 1, wherein the conductive layer is doped polycrystalline silicon.

Claim 6 (original): The method as claimed in claim 1, wherein the insulating barrier layer is SiN.

Claim 7 (original): The method as claimed in claim 1, wherein the dielectric layer comprises an oxide.

Claim 8 (original): The method as claimed in claim 1, wherein the dielectric layer comprises boro-phosphosilicate glass (BPSG).

Claim 9 (original): The method as claimed in claim 3, wherein the metal/metal compound layer comprises a Ti/TiSi layer.

Claim 10 (original): The method as claimed in claim 5, wherein the conductive layer is doped with an element in either group 13 (IIIA) or 15 (VA) of periodic table.

Claim 11 (original): The method as claimed in claim 5, wherein the conductive layer is doped with As.

Claim 12 (original) A method of a forming bit line contact via, comprising:

providing a substrate with a transistor thereon, the transistor having a gate electrode, drain region, and source region;

conformally forming a conductive layer overlying the substrate;

blanketly forming a doped polycrystalline silicon layer overlying the substrate;

removing the unwanted conductive layer and doped polycrystalline silicon layer, leaving the doped polycrystalline layer thinner than the gate electrode, overlying the drain region, and the conductive layer covered by the doped polycrystalline silicon layer;

conformally forming an insulating barrier layer overlying the substrate;

blanketly forming a dielectric layer overlying the insulating barrier layer; and

forming a via through the dielectric layer and insulating barrier layer, exposing the doped polycrystalline silicon layer.

Claim 13 (original): The method as claimed in claim 12, wherein removing the unwanted conductive layer and doped polycrystalline silicon layer further comprises:

removing a part of the doped polycrystalline silicon layer using etching or chemical mechanical polishing (CMP), thereby leaving the doped polycrystalline silicon layer, thinner than the gate electrode, overlying the drain region and source region;

forming a patterned resist layer exposing the doped polycrystalline silicon layer overlying the source region;

removing the exposed polycrystalline silicon layer using the patterned resist layer as a mask and the conductive layer as a stop layer, thereby exposing the conductive layer overlying the source region; and

removing the patterned resist layer and exposed conductive layer.

Claim 14 (original): The method as claimed in claim 12, wherein the conductive layer comprises a Ti/TiSi layer, and removing the unwanted conductive layer and doped polycrystalline silicon layer further comprises:

removing a part of the doped polycrystalline silicon layer using etching or chemical mechanical polishing (CMP), thereby leaving the doped polycrystalline silicon layer thinner than the gate electrode, overlying the drain region and source region;

forming a patterned resist layer exposing the doped polycrystalline silicon layer overlying the source region;

removing the exposed polycrystalline silicon layer using the patterned resist layer as a mask and the conductive layer as a stop layer, thereby exposing the conductive layer overlying the source region;

ashing the patterned resist layer using oxygen plasma; and

removing the exposed conductive layer using SPM (sulfuric acid-hydrogen peroxide mixture) and APM (ammonium hydrogen peroxide mixture).

Claim 15 (original): The method as claimed in claim 12, wherein the insulating barrier layer is SiN.

Claim 16 (original): The method as claimed in claim 12, wherein the dielectric layer comprises an oxide.

Claim 17 (original): The method as claimed in claim 12, wherein the dielectric layer comprises boro-phosphosilicate glass (BPSG).

Claim 18 (currently amended): The method as claimed in claim [[11]] 12, wherein the doped polycrystalline silicon layer is doped with an element in either group 13 (IIIA) or 15 (VA) of periodic table.

Claim 19 (currently amended): The method as claimed in claim [[11]] 12, wherein the doped polycrystalline silicon layer is doped with As.

Claim 20 (original) A method of a forming bit line contact via, comprising:

providing a substrate with a transistor thereon, the transistor having a gate electrode, drain region, and source region;

conformally forming a Ti/TiSi layer overlying the substrate;

blanketly forming a doped polycrystalline silicon layer overlying the substrate;

removing a part of the doped polycrystalline silicon layer, leaving the doped polycrystalline silicon layer thinner than the gate electrode, overlying the drain region and source region;

forming a patterned resist layer exposing the doped polycrystalline silicon layer overlying the source region;

removing the exposed polycrystalline silicon layer using the patterned resist layer as a mask and the Ti/TiSi layer as a stop layer, thereby exposing the Ti/TiSi layer overlying the source region;

ashing the patterned resist layer using oxygen plasma;

removing the exposed Ti/TiSi layer using SPM (sulfuric acid-hydrogen peroxide mixture) and APM (ammonium hydrogen peroxide mixture);

conformally forming an SiN layer overlying the substrate;

blanketly forming a dielectric layer overlying the SiN layer; and

forming a via through the dielectric layer and SiN layer, exposing the doped polycrystalline silicon layer.